11/13/03

SHEET 1 OF 1

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. MICRON.271A	APPLICATION NO. ~~Unknown~~ 10/712,212
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT Smith, et al.	
(USE SEVERAL SHEETS IF NECESSARY)	FILING DATE Herewith	GROUP ~~Unknown~~ 2815

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		*					

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		*						

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
OK	Yanagisawa, et al.; TRENCH TRANSISTOR CELL WITH SELF-ALIGNED CONTACT (TSAC) FOR MEGABIT MOS DRAM; 1st LSI Division, NEC Corporation; 1120 Shimokuzawa, Sagamihara, Kanagawa 229, Japan; Pages 132-135.
OK	Landgraf, et al.; SCALABLE HIGH VOLTAGE TRENCHGATE TRANSISTOR FOR FLASH; University of Regensburg, Conference: ESSDERC 2000; 93040 Regensburg, Germany; Pages 380-383.
OK	Hieda, et al.; SUB-HALF-MICROMETER CONCAVE MOSFET WITH DOUBLE LDD STRUCTURE; IEEE Transactions on Election Devices, Vol. 39, No. 3, March, 1992, Pages 671-676.
	Sakao, et al. A STRAIGHT-LINE TRENCH ISOLATION AND TRENCH-GATE TRANSISTOR (SLIT) CELL FOR GIGA-BIT DRAMS; ULSI Device Development Laboratories, NEC Corporation; 1120, Shimokuzawa, Sagamihara, Kanagawa 229, Japan; Pages 19 and 20. No date

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*/2000

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* No month cited.

EXAMINER	DATE CONSIDERED 2/8/05

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.